L Number	Hits	Search Text	DB	Time stamp
-	3	(6420271 6492271 5313633).pn.	USPAT	2004/07/01 10:52
_	ĺ	5923865.pn.	USPAT	2004/07/01 10:32
_	1 1	6130551.pn.	USPAT	2004/07/01 12:34
_	446	703/22.ccls.	USPAT;	2004/07/01 12:34
	440	703722.0013.	US-PGPUB;	2004/07/01 13.18
			EPO; JPO	
	23	702/22 cala and (EDCA on field adi		2004/07/01 13:19
-	2.3	703/22.ccls. and (FPGA or field adj	USPAT;	2004/07/01 13:19
		programmable adj gate adj array or	US-PGPUB;	
	1 1 1	programmable adj gate adj array)	EPO; JPO	0004/07/01 12 00
_	14	(703/22.ccls. and (FPGA or field adj	USPAT;	2004/07/01 13:23
		programmable adj gate adj array or	US-PGPUB;	
		programmable adj gate adj array)) and	EPO; JPO	
	277	emulat\$3		0001/07/03 10 00
_	377	703/23.ccls.	USPAT;	2004/07/01 13:23
			US-PGPUB;	
			EPO; JPO	İ
-	59	703/23.ccls. and (programmable adj gate	USPAT;	2004/07/01 13:23
		adj array or FPGA)	US-PGPUB;	
			EPO; JPO	
	30	(703/23.ccls. and (programmable adj gate	USPAT;	2004/07/01 14:05
		adj array or FPGA)) and (synthesiz\$4 or	US-PGPUB;	
	· .	map\$4)	EPO; JPO	
- :	2673	326/38-41.ccls.	USPAT;	2004/07/01 14:08
	İ		US-PGPUB;	
			EPO; JPO	
~	1022	326/38-41.ccls. and (programmable adj gate	USPAT;	2004/07/01 14:09
		adj array or FPGA)	US-PGPUB;	
			EPO; JPO	
_	275	(326/38-41.ccls. and (programmable adj	USPAT;	2004/07/01 14:10
		gate adj array or FPGA)) and (emulat\$3 or	US-PGPUB;	
		simulat\$3 or verification)	EPO; JPO	
-	158	((326/38-41.ccls. and (programmable adj	USPAT;	2004/07/01 14:11
		gate adj array or FPGA)) and (emulat\$3 or	US-PGPUB;	
		simulat\$3 or verification)) and (synthes\$4	EPO; JPO	1
		or map\$3 or compil\$2)		
_	87	(((326/38-41.ccls. and (programmable adj	USPAT;	2004/07/01 14:12
		gate adj array or FPGA)) and (emulat\$3 or	US-PGPUB;	
		simulat\$3 or verification)) and (synthes\$4	EPO; JPO	1
·		or map\$3 or compil\$2)) and (LUT or look		İ
:		adj up adj table)		
_	75		USPAT	2004/07/01 14:12
		gate adj array or FPGA)) and (emulat\$3 or	002111	
		simulat\$3 or verification)) and (synthes\$4		
		or map\$3 or compil\$2)) and (LUT or look		
		adj up adj table)) and logic		
_	75	(((((326/38-41.ccls. and (programmable adj	USPAT	2004/07/01 14:17
	'3	gate adj array or FPGA)) and (emulat\$3 or	20171	2004,07,01
		simulat\$3 or verification)) and (synthes\$4		
		or map\$3 or compil\$2)) and (LUT or look		
		adj up adj table)) and logic) and		
		(interconnect or rout\$3 or signal)		
	2	((((((326/38-41.ccls. and (programmable	USPAT	2004/07/01 14:17
		adj gate adj array or FPGA)) and (emulat\$3	OSPAI	2004/07/01 14:17
:		or simulat\$3 or verification)) and		
i				
		(synthes\$4 or map\$3 or compil\$2)) and (LUT		
		or look adj up adj table)) and logic) and		
		(interconnect or rout\$3 or signal)) and		
	000	log	HODE	0004/07/04 11:
-	980	716/4.ccls.	USPAT	2004/07/01 14:40
-	80	716/4.ccls. and (FPGA or field adj	USPAT	2004/07/01 14:41
		programmable adj gate adj array)		000.45= 455
-	59	(716/4.ccls. and (FPGA or field adj	USPAT	2004/07/01 14:41
		programmable adj gate adj array)) and		
		(emulat\$3 or simulat\$3)		
-	46	1 , , , , , , , , , , , , , , , , , , ,	USPAT	2004/07/01 14:42
		programmable adj gate adj array)) and		
		(emulat\$3 or simulat\$3)) and (synthesi\$3		
		or map\$3)		

-	46	(((716/4.ccls. and (FPGA or field adj	USPAT	2004/07/01 14:50
1		programmable adj gate adj array)) and		
		(emulat\$3 or simulat\$3)) and (synthesi\$3		
	251	or map\$3)) and logic 716/13.ccls.	USPAT	2004/07/01 14:50
_	13	716/13.ccls. and (FPGA or field adj	USPAT	2004/07/01 14:51
	13	programmable adj gate adj array)		
_	5	(716/13.ccls. and (FPGA or field adj	USPAT	2004/07/01 14:54
		programmable adj gate adj array)) and		
		(emulat\$3 or simulat\$3)		0004/07/01 14-54
-	381	716/17.ccls.	USPAT USPAT	2004/07/01 14:54 2004/07/01 14:54
-	141	716/17.ccls. and (FPGA or programmable adj	USPAI	2004/07/01 14:54
	68	gate adj array) (716/17.ccls. and (FPGA or programmable	USPAT	2004/07/01 14:55
_	00	adj gate adj array)) and (emulat\$3 or	002111	
		simulat\$3)		
_	51	((716/17.ccls. and (FPGA or programmable	USPAT	2004/07/01 14:55
		adj gate adj array)) and (emulat\$3 or		
		simulat\$3)) and (synthesi\$3 or map\$3)		0004/07/04 45 00
-	11	(((716/17.ccls. and (FPGA or programmable	USPAT	2004/07/01 15:00
		adj gate adj array)) and (emulat\$3 or		
		<pre>simulat\$3)) and (synthesi\$3 or map\$3)) and LUT</pre>		
_	562	716/18.ccls.	USPAT	2004/07/01 15:00
	118	716/18.ccls. and (fpga or programmable adj	USPAT	2004/07/01 15:01
	110	logic adj device)		
-	74	(716/18.ccls. and (fpga or programmable	USPAT	2004/07/01 15:01
		adj logic adj device)) and (emulat\$3 or		
	_	simulat\$3)	HODAM	2004/07/01 15:02
-	9	(((716/18.ccls. and (fpga or programmable adj logic adj device)) and (emulat\$3 or	USPAT	2004/07/01 13:02
		simulat\$3)) and (synthesi\$3 or map\$3)) and		
1		(LUT or look adj up adj table)		
_	67	((716/18.ccls. and (fpga or programmable	USPAT	2004/07/01 15:02
		adj logic adj device)) and (emulat\$3 or		
		simulat\$3)) and (synthesi\$3 or map\$3)		
_	19	synthesis and logic and emulation and	USPAT	2004/07/01 15:24
		programmable adj gate adj array and signal		
		and physical and (storage adj unit or lut		
	408	or look adj up adj table) 716/16.ccls.	USPAT;	2004/07/02 15:24
-	400	710710.0013.	US-PGPUB;	
			EPO; JPO	
_	275	716/16.ccls. and (PLD or FPGA)	USPAT;	2004/07/02 14:25
			US-PGPUB;	
			EPO; JPO	2004/07/02 14:05
_	69	(716/16.ccls. and (PLD or FPGA)) and	USPAT;	2004/07/02 14:25
		partitioning	US-PGPUB; EPO; JPO	
	61	((716/16.ccls. and (PLD or FPGA)) and	USPAT;	2004/07/02 14:25
1-	ΘŢ	partitioning) and multiple	US-PGPUB;	
		pareterining, and maretpro	EPO; JPO	
_	683	716/18.ccls.	USPAT;	2004/07/02 15:25
			US-PGPUB;	
	1		EPO; JPO	0004/07/00 == ==
_	145	716/18.ccls. and (PLD or FPGA)	USPAT;	2004/07/02 15:25
		4	US-PGPUB; EPO; JPO	
	7.	(716/18.ccls. and (PLD or FPGA)) and	USPAT;	2004/07/02 15:25
_	75	partition\$3	US-PGPUB;	2001,01,02 10.20
		pareternity	EPO; JPO	
_	68	((716/18.ccls. and (PLD or FPGA)) and	USPAT;	2004/07/02 15:44
		partition\$3) and multiple	US-PGPUB;	
			EPO; JPO	0004/07/22 25 15
-	1027	716/5.ccls.	USPAT;	2004/07/02 15:45
			US-PGPUB; EPO; JPO	
	71	716/5.ccls. and (PLD or FPGA)	USPAT;	2004/07/02 15:45
	'1	/10/3.CC13. and (FDD OI IIGA)	US-PGPUB;	
			EPO; JPO	
	J	1		

-	25	(716/5.ccls. and (PLD or FPGA)) and	USPAT;	2004/07/02 15:51
		partition\$3	US-PGPUB;	
			EPO; JPO	
-	404	716/7.ccls.	USPAT;	2004/07/02 15:51
	ļ		US-PGPUB;	
_	63	716/7 1- and (DID DDOD)	EPO; JPO	
_	63	716/7.ccls. and (PLD or FPGA)	USPAT;	2004/07/02 15:51
			US-PGPUB;	l i
_	53	(716/7.ccls. and (PLD or FPGA)) and	EPO; JPO	2004/07/02 15 51
İ	33	partition\$3	USPAT; US-PGPUB;	2004/07/02 15:51
		parereionys	EPO; JPO	
_	50	((716/7.ccls. and (PLD or FPGA)) and	USPAT;	2004/07/02 15:52
		partition\$3) and multiple	US-PGPUB;	2004/01/02 13.32
		*	EPO; JPO	
-	206	i i i i i i i i i i i i i i i i i i i	USPAT	2004/07/06 10:01
		adj logic or multiple adj value adj logic		
		or multiple-valued adj logic		
-	8	(multi-value adj logic or multi adj value	USPAT	2004/07/06 10:02
		adj logic or multiple adj value adj logic		
		or multiple-valued adj logic) and FPGA	<u> </u>	

APP # 09779859

7/1/04

Inventor Name Search: EAST, IEEE, ACM, GOOGLE

7/2/04

Talked to Bill Thomson, PRI AU2123

Talked to Kevin Teska, SPE 2123

ACM

+partition +synthesize +logic +LUT +table FPGA PLD

7/6/04

TEEE:

fpga<and>multi value <or>multiple valued

fpga<and>multiple value<and>synthesis

Proceedings 1999 29th IEEE International Symposium on Multiple-Valued Logic (Cat. No.99CB36329)

Proceedings. 1998 28th IEEE International Symposium on Multiple Valued Logic (Cat. No.98CB36138)

Proceedings 1997 27th International Symposium on Multiple- Valued Logi

Proceedings of 26th IEEE International Symposium on Multiple-Valued Lo qic (ISMVL'96)

Year: 23-25 May 1995

Proceedings 25th International Symposium on Multiple-Valued Logic Multiple-Valued Logic, 1994. Proceedings., Twenty-Fourth International Symposium on

ACM

+fpga, +lut, +emulate "multiple-valued logic", "multi-value logic"
+"multiple-valued logic" fpga emulate

7/7/04

google: hamlet, programmable, "multiple-valued"

ACM: +author:butler +author:j